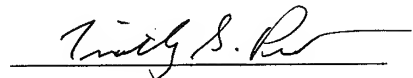


VERIFICATION OF TRANSLATION

I, Timothy S. Price, translator at Nakajima & Matsumura Patent Attorneys Office, 6F Yodogawa 5-Bankan, 3-2-1 Toyosaki, Kita-ku, Osaka, 531-0072, Japan, hereby declare that I am conversant with the English and Japanese languages and am a competent translator thereof. I further declare that to the best of my knowledge and belief the following is a true and correct translation made by me of a Japanese Patent Application No. 2003-305402 filed on August 28, 2003.

Date: January 25, 2008

A handwritten signature in cursive script, reading "Timothy S. Price", written over a horizontal line.

Timothy S. Price

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[RECEIPT NO.] 014823

[AMOUNT] ¥21,000

20 [LIST OF ENCLOSURES]

Claims 1

Specification 1

Drawings 1

Abstract 1

25 [POWER OF ATTORNEY NO.] 9003742

[DOCUMENT] Claims

[CLAIM 1]

A semiconductor light emitting device comprising:

a substrate;

5 a semiconductor multilayer film formed over a main surface of the substrate by crystal growth, the semiconductor multilayer film including a first conductive layer, a light emitting layer, and a second conductive layer in the stated order beginning on a substrate side, a removed multilayer portion having been formed along
10 an outer circumference of the main surface, the removed multilayer portion having been formed by removing a portion of the semiconductor multilayer film from an outermost layer thereof to at least the first conductive layer; and

a phosphor film covering a side surface of the semiconductor
15 multilayer film that faces the removed multilayer portion, and a main surface of the outermost layer.

[CLAIM 2]

The semiconductor light emitting device of claim 1, wherein
20 the semiconductor multilayer film further includes a reflective layer which is formed between the substrate and the first conductive layer.

[CLAIM 3]

25 The semiconductor light emitting device of claim 2, wherein

the reflective layer is made of an AlGaIn semiconductor.

[CLAIM 4]

A semiconductor light emitting device according to any of claims 1 to 3, further comprising:

5 a first electrode that is formed on the first conductive layer;

 a second electrode that is formed on the second conductive layer;

 a first power supply terminal and a second power supply
10 terminal that are formed on a main surface of the substrate which faces away from the semiconductor multilayer film;

 a first conductive member including a first through hole that is provided in the substrate, and electrically connecting the first electrode and the first power supply terminal; and

15 a second conductive member including a second through hole that is provided in the substrate, and electrically connecting the second electrode and the second power supply terminal.

[CLAIM 5]

20 The semiconductor light emitting device of claim 4, wherein the removed multilayer portion has been formed by removing a portion of the semiconductor multilayer film that includes all layers, such that the substrate is exposed, and

 the first through hole and the second through hole are
25 provided in a portion of the substrate that corresponds to the removed multilayer portion.

[CLAIM 6]

A semiconductor light emitting device according to any of claims 1 to 5, wherein

the substrate is made of one of SiC, AlN, GaN, BN, and Si.

5

[CLAIM 7]

A semiconductor light emitting device according to any of claims 1 to 6, wherein

the main surface of the semiconductor multilayer film on
10 a same side as a light extraction side of the light emitting layer
is uneven.

[CLAIM 8]

A semiconductor light emitting device according to any of
15 claims 1 to 7, wherein

light emitted from the light emitting layer has a wavelength
component within a range of 380 nm to 780 nm.

[CLAIM 9]

20 A light emitting module comprising:
a printed-wiring board; and
a semiconductor light emitting device as in any of claims
1 to 8, having been mounted on the printed-wiring board.

25 [CLAIM 10]

A lighting apparatus including, as a light source, a light
emitting module as in claim 9.

[CLAIM 11]

A manufacturing method for a semiconductor light emitting device, comprising:

5 a first step of forming a semiconductor multilayer film including a light emitting layer on a main surface of a substrate by crystal growth;

 a second step of dividing the semiconductor multilayer film into a plurality of portions by removing a part of the semiconductor
10 multilayer film so as that an area of the main surface of the substrate is externally exposed;

 a third step of forming a phosphor film that covers the exposed area of the main surface of the substrate and all exposed surfaces of each of the plurality of portions; and

15 a fourth step of dicing the substrate according to each of the plurality of portions.

[DOCUMENT] Detailed Description of the Invention

[TITLE OF THE INVENTION] Semiconductor Light Emitting Device, Light
Emitting Module, Lighting Apparatus, and Manufacturing Method for
5 Semiconductor Light Emitting Device

[FIELD OF THE INVENTION]

[0001]

The present invention relates to a semiconductor light
10 emitting device such as a light emitting diode chip (LED chip), and
also to a light emitting module and a lighting apparatus using the
semiconductor light emitting device, and a manufacturing method for
the semiconductor light emitting device. The present invention
particularly relates to a semiconductor light emitting device that
15 emits visible light of a desired color using a phosphor.

[DESCRIPTION OF THE RELATED ART]

[0002]

LEDs have a higher efficiency and a longer lifetime than
20 incandescent lamps and halogen lamps. In the field of LEDs, vigorous
research has recently been conducted to use white LEDs for lighting,
as white LEDs with higher luminance have been developed. A common
white LED at present includes a combination of an LED bare chip emitting
blue light and a phosphor excited by the blue light to emit yellow
25 light, so that the blue light and the yellow light mix together to
generate white light.

[0003]

A manufacturing method for this white LED includes a wafer fabrication process in which the LED bare chip is obtained and an assembly process in which the LED bare chip is packaged.

[0004]

5 In the assembly process, the LED bare chip is mounted on a lead frame, a printed-wiring board or the like since the LED bare chip alone can not be put to use. After this, a resin mixed with a phosphor material is dropped onto the mounted LED bare chip and cured, to form a phosphor film. Subsequently, steps such as molding
10 a periphery of the phosphor film using a resin are conducted to complete the white LED. The completed white LED is tested for its electrical and optical performance before shipped.

[0005]

 However, there is a high possibility that the white LED
15 manufactured in the above-described manner has poor optical performance. The reason is explained in the following. Firstly, the phosphor film is formed in such a manner that the resin mixed with the phosphor material is dropped onto the LED bare chip and then cured. Therefore, it is highly likely that the thickness of the
20 phosphor film in the white LED is not equal to a designed thickness. Here, a color temperature of the white light emitted by the white LED is determined by a ratio between a quantity of the blue light and a quantity of the yellow light. This being so, if the phosphor
25 film is thick, the quantity of the blue light is small and the quantity of the yellow light is large, so that white light of a low color temperature is produced. On the other hand, if the phosphor film is thin, white light of a high color temperature is produced.

Consequently, a desired color temperature can not be realized. Secondly, the phosphor film tends to be formed at an uneven thickness. If the phosphor film is formed at an inappropriately uneven thickness, unevenness of color occurs.

5 [0006]

White LEDs with the above-mentioned defects are rejected as a result of the optical performance test. This results in a low ratio of accepted finished products (white LEDs) to all finished products.

10 [0007]

In an attempt to improve the ratio of accepted finished products, it has been proposed to test white LEDs for unevenness of color prior to the assembly process. This proposal has been realized by an LED chip that is disclosed in patent document 1.

15 [0008]

According to patent document 1, an LED bare chip is mounted on a substrate (an auxiliary mounting element) that has a larger surface area than the LED bare chip, and a phosphor film is then formed on and around the LED bare chip mounted on the auxiliary mounting substrate. Thus, this LED bare chip can be tested for its optical performance prior to an assembly process in which the LED bare chip is mounted on a lead frame or a printed-wiring board. As a consequence, the ratio of accepted finished products can be improved.

[PATENT DOCUMENT 1] Japanese Patent Application Publication
25 No. 2001-15817 (Japanese Patent No. 3399440)

[DISCLOSURE OF THE INVENTION]

[PROBLEMS THE INVENTION IS GOING TO SOLVE]

[0009]

However, the LED chip disclosed in patent document 1 requires the provision of an extra constituent, i.e. the auxiliary mounting
5 element, and also has an extra step for mounting the LED bare chip to the auxiliary mounting element.

[0010]

In light of the above-described problems, an object of the present invention is to provide a semiconductor light emitting device
10 which can be tested for its optical performance before being packaged, without increasing the number of constituents or manufacturing steps. The object includes provision of a manufacturing method for the semiconductor light emitting device, and a light emitting module and a lighting apparatus using the semiconductor light emitting
15 device.

[MEANS TO SOLVE THE PROBLEMS]

[0011]

In order to achieve the above object, the present invention
20 is a semiconductor light emitting device including: a substrate; a semiconductor multilayer film formed over a main surface of the substrate by crystal growth, the semiconductor multilayer film including a first conductive layer, a light emitting layer, and a second conductive layer in the stated order beginning on a substrate
25 side, a removed multilayer portion having been formed along an outer circumference of the main surface, the removed multilayer portion having been formed by removing a portion of the semiconductor

multilayer film from an outermost layer thereof to at least the first conductive layer; and a phosphor film covering a side surface of the semiconductor multilayer film that faces the removed multilayer portion, and a main surface of the outermost layer.

5 [0012]

Also, the semiconductor multilayer film may further include a reflective layer which is formed between the substrate and the first conductive layer.

[0013]

10 Furthermore, the reflective layer may be made of an AlGaN semiconductor.

[0014]

Also, the above semiconductor light emitting device may further include: a first electrode that is formed on the first
15 conductive layer; a second electrode that is formed on the second conductive layer; a first power supply terminal and a second power supply terminal that are formed on a main surface of the substrate which faces away from the semiconductor multilayer film; a first conductive member including a first through hole that is provided
20 in the substrate, and electrically connecting the first electrode and the first power supply terminal; and a second conductive member including a second through hole that is provided in the substrate, and electrically connecting the second electrode and the second power supply terminal.

25 Also, the removed multilayer portion may have been formed by removing a portion of the semiconductor multilayer film that includes all layers, such that the substrate is exposed, and the

first through hole and the second through hole may be provided in a portion of the substrate that corresponds to the removed multilayer portion.

[0015]

5 Also, the substrate may be made of one of SiC, AlN, GaN, BN, and Si.

[0016]

 Also, the main surface of the semiconductor multilayer film on a same side as a light extraction side of the light emitting layer
10 may be uneven.

[0017]

 Also, light emitted from the light emitting layer may have a wavelength component within a range of 380 nm to 780 nm.

[0018]

15 In order to achieve the above object, the present invention is also a light emitting module including: a printed-wiring board; and the above semiconductor light emitting device, having been mounted on the printed-wiring board.

[0019]

20 In order to achieve the above object, the present invention is also a lighting apparatus including, as a light source, the above light emitting module.

 In order to achieve the above object, the present invention is also a manufacturing method for a semiconductor light emitting
25 device, including: a first step of forming a semiconductor multilayer film including a light emitting layer on a main surface of a substrate by crystal growth; a second step of dividing the semiconductor

multilayer film into a plurality of portions by removing a part of the semiconductor multilayer film so as that an area of the main surface of the substrate is externally exposed; a third step of forming a phosphor film that covers the exposed area of the main surface of the substrate and all exposed surfaces of each of the plurality of portions; and a fourth step of dicing the substrate according to each of the plurality of portions.

[EFFECTS OF THE INVENTION]

10 [0020]

The semiconductor light emitting device of the present invention includes a semiconductor multilayer film formed over a main surface of the substrate by crystal growth, the semiconductor multilayer film including a first conductive layer, a light emitting layer, and a second conductive layer in the stated order beginning on a substrate side, a removed multilayer portion having been formed along an outer circumference of the main surface, the removed multilayer portion having been formed by removing a portion of the semiconductor multilayer film from an outermost layer thereof to at least the first conductive layer; and a phosphor film covering a side surface of the semiconductor multilayer film that faces the removed multilayer portion, and a main surface of the outermost layer. According to this construction, the semiconductor light emitting device can be tested for its optical performance, such as unevenness of color. That is to say, the semiconductor light emitting device can be tested before mounting on a lead frame or a printed-wiring board. In this way, a ratio of accepted finished products to all

finished products can be improved without requiring an additional member such as an auxiliary mounting element as in the related art.

[0021]

Also, the light emitting module and the lighting device
5 of the present invention include the above semiconductor light emitting device. In this way, a ratio of accepted finished products to all finished products can be improved, thereby enabling a reduction in cost.

[0022]

Also, in the manufacturing method for the semiconductor
10 light emitting device of the present invention, the semiconductor multilayer film is divided into a plurality of portions by removing a part of the semiconductor multilayer film so as that an area of the main surface of the substrate is externally exposed, and there
15 is formed a phosphor film that covers the exposed area of the main surface of the substrate and all exposed surfaces of each of the plurality of portions. This method enables achieving the above-described effects.

20 [EMBODIMENT OF THE INVENTION]

[0023]

The following describes an embodiment of the present invention with reference to the drawings.

[0024]

25 Fig.1A is an external perspective view illustrating a construction of an LED array chip 2, which is one type of a semiconductor light emitting device, and Fig.1B is a plan view

illustrating the LED array chip 2. Fig.1A mainly illustrates how LEDs 6 (mentioned later) are arranged in the LED array chip 2, and therefore does not show minute depressions and protrusions on surfaces of the LEDs 6. Fig.1B illustrates the LED array chip after
5 removing a phosphor film 48 (mentioned later).

[0025]

As shown in Figs.1A and 1B, the LED array chip 2 is formed in such a manner that the LEDs 6 are arranged in a matrix of N rows and M columns (in the present embodiment, a matrix of seven rows
10 and five columns, in total, 35 LEDs 6) on a non-doped (highly resistive) SiC substrate 4 which is a semiconductor substrate (hereinafter simply referred to as "an SiC substrate 4"). The LEDs 6 are light emitting elements each of which is formed by a semiconductor multilayer film including a light emitting layer. The 35 LEDs 6 are
15 formed by crystal growth on a main surface of the SiC substrate 4 with a space having a width (W_4) of 50 μm being left. The space is an area of the main surface of the SiC substrate 4 in which a semiconductor multilayer film (the 35 LEDs 6) is not formed. In other words, the space is formed so as to surround the semiconductor
20 multilayer film. The space is hereinafter referred to as an exposed portion 7.

A size $L_1 \times W_1$ of each LED 6 is 285 $\mu\text{m} \times 400 \mu\text{m}$. A size $L_2 \times W_2$ of an area in which the LEDs 6 are formed is 2 mm \times 2 mm. A size $L_3 \times W_3$ of the LED array chip 2 is 2.1 mm \times 2.1 mm.

25

[0026]

The following part describes, in more detail, the construction of the LED array chip 2 with reference to cross-sectional

views.

[0027]

Fig.2A illustrates a cross-section of the LED array chip 2 along a line AA shown in Fig.1B, and Fig, 2B illustrates a cross-section of the LED array chip 2 along a line BB shown in Fig.1B. Specifically speaking, Fig.2A illustrates a cross-section of an LED 6a of the first row and the first column and an LED 6b of the first row and the second column, and Fig.2B illustrates a cross-section of an LED 6c of the seventh row and the third column and an LED 6d of the seventh row and the fifth column.

[0028]

Each LED 6 is formed by a semiconductor multilayer film made up of an n-AlGa_N buffer layer 8 (having a thickness of 30 nm), a distributed bragg reflector (DBR) layer 10 composed of 30 periods of n-AlGa_N/Ga_N (having a total thickness of 3 μm), an n-Ga_N clad layer 12 (having an Si-doping amount of $3 \times 10^{18} \text{ cm}^{-3}$ and a thickness of 200 nm), an InGa_N/Ga_N multiple quantum well (MQW) light emitting layer 14 composed of six periods of InGa_N (having a thickness of 2 nm)/Ga_N (having a thickness of 8 nm), a p-Ga_N clad layer 16 (having an Mg-doping amount of $1 \times 10^{19} \text{ cm}^{-3}$ and a thickness of 200 nm), and a p-Ga_N contact layer 18 (having an Mg-doping amount of $3 \times 10^{19} \text{ cm}^{-3}$ and a thickness of 200 nm). These layers 8, 10, 12, 14, 16 and 18 are formed on the SiC substrate 4 in the stated order. Which is to say, the LED 6 basically has a construction in which a light emitting layer (the MQW light emitting layer 14) is sandwiched between a conductive layer (the n-Ga_N clad layer 12 on a side of the SiC substrate 4) and a conductive layer (the p-Ga_N contact layer 18 and the p-Ga_N

clad layer 16 on a side of a light extraction surface).

An Ni/Au thin film 20 and an ITO transparent electrode 22 are formed on the p-GaN contact layer 18 in this order. A Ti/Au electrode 24, which is an n-electrode, is formed on the n-GaN clad layer 12.

[0029]

When power is supplied to this LED 6 through the ITO transparent electrode 22 and the Ti/Au electrode 24, the light emitting layer 14 emits blue light having a wavelength of 460 nm. The Ni/Au thin film 20 and the ITO transparent electrode 22 are used as a p-electrode in the present embodiment to improve transmission of the light emitted from the light emitting layer 14.

[0030]

A main surface of the p-electrode of the LED 6 from which light is extracted is made regularly uneven in order to improve light extraction efficiency. To be more specific, as shown in Fig. 3A, which is a plan view illustrating the LED 6, circular depressions 25 are formed at a predetermined interval (d) of 1 μ m in the present embodiment. Here, a planar shape of each depression 25 is not limited to a circle as described above, but may be a quadrangle or a hexagon. Furthermore, the uneven surface may be achieved by creating linear grooves at a predetermined interval, or simply by irregularly damaging the surface of the p-electrode.

[0031]

The 35 LEDs 6 described above are connected in series on the SiC substrate 4.

[0032]

Figs.2A and 2B are used to explain how the LEDs 6 are connected in the LED array chip 2.

[0033]

As shown in Fig.2A, the adjacent LEDs 6a and 6b are divided from each other by a division groove 26 that is deep enough to reach the SiC substrate 4. The same holds true for all pairs of adjacent LEDs 6 including the LEDs 6c and 6d shown in Fig.2B.

[0034]

An insulating film (Si_3N_4 film) 28 is formed so as to cover side surfaces of each of the LEDs 6a, 6b, 6c and 6d and the division grooves 26. A bridging wire 30 is formed on the insulating film 28 to connect a p-electrode of the LED 6a (an Ni/Au thin film 20 and an ITO transparent electrode 22) to an n-electrode of the LED 6b (a Ti/Au electrode 24). Similarly, another bridging wire 30 formed on the insulating film 28 connects a p-electrode of the LED 6c and an n-electrode of the LED 6d as shown in Fig.2B. In the same manner, bridging wires 30 connect LEDs 6 from an LED 6e of the first row and the third column to an LED 6f of the seventh row and the third column. As a result, all of the LEDs 6 are connected in series as shown in Fig.3B. Among the 35 LEDs 6 connected in series in the LED array chip 2, the LED 6a is an LED on a lower potential end of the LED array chip 2. Therefore, a Ti/Au electrode 24 of the LED 6a is a cathode electrode 32 of the LED array chip 2. The LED 6d is an LED on a higher potential end. Therefore, an Ni/Au thin film 20 and an ITO transparent electrode 22 of the LED 6d are an anode electrode 34 of the LED array chip 2.

[0035]

Fig.3C illustrates a back surface of the LED array chip 2. As shown in Fig.3C, two power supply terminals 36 and 38 are formed on the back surface, which is opposite to a front surface of the SiC substrate 4 on which the LEDs 6 are formed. The power supply
5 terminals 36 and 38 are each formed by a Ti/Pt/Au film.

[0036]

As shown in Figs.2A and 2B, the cathode electrode 32 is connected to the power supply terminal 36 by a bridging wire 40 and a through hole 42 provided in the SiC substrate 4, and the anode
10 electrode 34 is connected to the power supply terminal 38 by a bridging wire 44 and a through hole 46 provided in the SiC substrate 4. The through holes 42 and 46 are each formed by filling an opening with a diameter of 30 μm provided in the SiC substrate 4 with Pt. When an electric current of 50 mA is supplied to the 35 LEDs 6 connected
15 in series through the power supply terminals 36 and 38 with heat dissipation being ensured, an operation voltage of 120V is observed.

[0037]

The phosphor film 48 is formed on the front surface of the SiC substrate 4 so as to cover the LEDs 6 and the entire exposed
20 portion 7 of the SiC substrate 4. The phosphor film 48 is made of a light-transmitting resin, for example, silicone in which particles of a yellow phosphor $(\text{Sr}, \text{Ba})_2\text{SiO}_4:\text{Eu}^{2+}$ and fine particles of SiO_2 are dispersed. The phosphor film 48 has a thickness T (shown in Fig.2A) of 50 μm . The light-transmitting resin may be an epoxy resin or a
25 polyimide resin, instead of silicone.

[0038]

The phosphor in the phosphor film 48 converts part of the

blue light emitted from the light emitting layer 14 of each LED 6 into yellow light. Here, the blue light from each LED 6 and the yellow light from the phosphor mix together, to generate white light. Since the DBR layer 10, which is a light reflective layer, is formed between the light emitting layer 14 and the SiC substrate 4, 99% or more of blue light emitted from the light emitting layer 14 towards the SiC substrate 4 is reflected towards the light extraction surface. This improves light extraction efficiency of each LED 6. It should be noted that blue light indicates light having a wavelength from 400 nm inclusive to 500 nm exclusive, and yellow light indicates light having a wavelength from 550 nm inclusive to 600 nm exclusive, in this description. Taking this into consideration, the LEDs 6 may be configured to emit light having a peak emission wavelength that falls within the above-mentioned range, instead of a peak emission wavelength of 460 nm as described above.

[0039]

The following part describes a manufacturing method for the LED array chip 2 described above, with reference to Figs.4, 5 and 6.

[0040]

In Figs.4, 5 and 6, a material to form each constituent of the LED array chip 2 is identified by a three-digit number whose first digit is one. The last two digits of the three-digit number represents a reference numeral identifying the corresponding constituent of the LED array chip 2.

[0041]

Firstly, as shown in Fig.4, an n-AlGaIn buffer layer 108,

a DBR layer 110 composed of 30 periods of n-AlGa_N/Ga_N, an n-Ga_N clad layer 112, an InGa_N/Ga_N MQW light emitting layer 114, a p-Ga_N clad layer 116 and a p-Ga_N contact layer 118 are formed on a non-doped SiC substrate 104 in the stated order using a metal organic chemical vapor deposition (MOCVD) method (step A). Here, the non-doped SiC substrate 104 has a diameter of two inches and a thickness of 300 μm .

[0042]

After this, a mask 50 is formed, so as to mask an area, on the lamination made up of the layers 118, 116, 114, 112, 110 and 108, that is slightly larger than an area in which the Ni/Au thin film 20 (and the ITO transparent electrode 22) of each LED 6 is to be formed. An unmasked area of the lamination is removed by etching to a depth of approximately half of the thickness of the n-Ga_N clad layer 112 is removed (step B). Thus, a surface to connect the Ti/Au electrode 24 (an n-electrode formation surface) 52 is formed. The mask 50 is removed prior to the next step.

[0043]

After this, a mask 54 is formed so as to cover the resulting surface after the step B except for areas in which the exposed portion 7 and the division groove 26 are to be formed. Unmasked areas of a lamination made up of the remaining layer 112 and the layers 110 and 108 are removed by etching to such a depth that the SiC substrate 104 is exposed, to create the exposed portion 7 and the division groove 26 (step C). Which is to say, the exposed portion 7 is created by removing a corresponding part of the semiconductor multilayer film composed of the layers 108 to 118 (the corresponding part of

the semiconductor multilayer film which has been removed is hereinafter referred to as a removed multilayer portion.). After the etching is performed, the mask 54 is removed prior to the next step.

5 [0044]

An Si_3N_4 film 128, which is an insulating film, is formed by sputtering or the like for insulation and surface protection (step D).

[0045]

10 A mask 56 is then formed so as to mask the Si_3N_4 film 128 except for an area in which the Ni/Au thin film 20 (and the ITO transparent electrode 22) of each LED 6 is to be formed. An unmasked area of the Si_3N_4 film 128 is removed by etching, and an Ni/Au thin film 120 is then formed by deposition. Thus, the Ni/Au thin film
15 20 is formed (step E). A portion of the Ni/Au thin film 120 which is formed on the mask 56 (no shown in Fig.5) is removed together with the mask 56 prior to the next step.

[0046]

The same procedure as in the step E is conducted to form
20 the Ti/Au electrode 24. Specifically speaking, a mask 58 is formed so as to mask the resulting surface after the step E, except for an area on the Si_3N_4 film 128 in which the Ti/Au electrode 24 for each LED 6 is to be formed. After an unmasked area of the Si_3N_4 film 68 is removed by etching, a Ti/Au film 124, which is a thin metal
25 film, is applied by deposition. Thus, the Ti/Au electrode 24 is formed (step F). A portion of the Ti/Au film 124 which is formed on the mask 58 (not shown in Fig.5) is removed together with the mask 58

prior to the next step.

[0047]

After this, a mask 60 is formed so as to cover the resulting surface after the step F except for an area in which the through
5 holes 42 and 46 are to be formed. An unmasked area of the resulting surface is removed by etching, to form an opening 61 having a depth of 200 μm . Then, the opening 61 is filled with Pt by electroless deposition or the like (step G). The mask 60 is removed prior to the next step.

10 [0048]

Subsequently, a mask 62 is formed to mask the resulting surface after the step G except for areas in which the depressions 25 are to be formed. Unmasked areas of the resulting surface are removed by etching to such a depth that the p-GaN contact layer 118
15 is exposed, to form the depressions 25 (step H). The mask 62 is removed prior to the next step.

[0049]

After this, a mask 64 is formed so as to mask the resulting surface after the step H except for an area in which the ITO transparent
20 electrode 22 of each LED 6 is to be formed. Then, an ITO film 122 is applied by sputtering, to form the ITO transparent electrode 22 for each LED 6 (step I). A portion of the ITO film 122 which is formed on the mask 64 (not shown in Fig.6) is removed together with the mask 64 prior to the next step.

25 [0050]

~~In the next step, the bridging wires 30, 40 and 44 are formed~~
in the following manner. A mask 66 is formed so as to mask the resulting

surface after the step I, except for areas in which the bridging wires 30, 40 and 44 are to be formed. Then, a Ti/Pt/Au film, which is a thin metal film, is applied by deposition, to form the bridging wires 30, 40 and 44 (step J). A portion of the Ti/Pt/Au film which
5 is formed on the mask 66 (not shown in Fig.7) is removed together with the mask 66 prior to the next step.

After this, a back surface of the SiC substrate 104 is polished so that the thickness of the SiC substrate 104 becomes 150 μm . Thus, the through holes 42 and 46 are exposed on the back surface
10 of the SiC substrate 104 (step K).

Subsequently, a mask (not shown in Fig.7) is formed so as to mask the back surface of the SiC substrate 104 except for areas in which the power supply terminals 36 and 38 are to be formed. After this, a Ti/Pt/Au film, which is a thin metal film, is applied by
15 deposition. Thus, the Ti/Pt/Au power supply terminals 36 and 38 are formed (step L). A portion of the Ti/Pt/Au film which is formed on the mask (not shown in Fig.7) is removed together with the mask prior to the next step.

After this, silicone in which particles of a yellow phosphor
20 $(\text{Sr}, \text{Ba})_2\text{SiO}_4:\text{Eu}^{2+}$ and fine particles of SiO_2 are dispersed is applied by printing so as to cover the exposed portion 7 and the LEDs 6. The silicone is heated to be cured, to form the phosphor film 48. Subsequently, the phosphor film 48 is polished so that the thickness of the phosphor film 48 becomes 50 μm (step M). Here, it should be
25 noted that color of white light emitted from the LED array chip 2 is determined by a ratio between blue light emitted from the LEDs 6 and yellow light generated by converting the blue light. This ratio

can be adjusted by changing the percentage of the phosphor particles included in the silicone resin and the thickness of the phosphor film 48. Specifically speaking, when the percentage of the phosphor particles is higher, or the thickness of the phosphor film 48 is larger, the ratio of the yellow light becomes higher. Here, a high ratio of the yellow light means that the white light has a low color temperature. According to the present embodiment, the silicone resin including the phosphor particles is first applied at a thickness larger than a designed thickness of the phosphor film 48. The applied resin is then polished after heated to be cured, to achieve the designed thickness. In this way, the phosphor film 48 can be formed at an even thickness. This reduces unevenness of color with it being possible to produce white light having a predetermined color temperature reliably.

Lastly, the SiC substrate 104 is divided into individual LED array chips 2 by dicing, to obtain the LED array chip 2 (shown in Figs. 1A and 1B).

[0051]

Here, the phosphor film may be formed by applying a resin including a phosphor after a mesa etching step but before a dicing step in a conventional wafer fabrication process. However, a groove created by conventional mesa etching has such a width that only one or two phosphor particles can be arranged in a widthwise direction. In this case, blue light emitted from side surfaces of the light emitting layer of each LED, to a large extent, goes through the phosphor layer without exciting the phosphor. As a result, the blue light emitted from the side surfaces becomes noticeable, which causes

unevenness of color. According to the present embodiment, however, the resin including the phosphor is applied on side surfaces of the semiconductor multilayer film (the side surfaces of the light emitting layer) at a thickness having an equal length to the width
5 of the exposed portion. Here, the width of the exposed portion is sufficiently larger than a diameter of the phosphor particle. As a consequence, the blue light emitted from the side surfaces of the light emitting layer can appropriately excites the phosphor to be converted into yellow light. This reduces unevenness of color.

10 [0052]

It is generally accepted that unevenness of color occurs only in a white LED that uses visible light having a spectral component of a wavelength within a range of 380 nm and 780 nm (purple to red) for an excitation light source. In other words, unevenness of color
15 does not occur in a white LED having near-ultraviolet light as an excitation light source. However, ultraviolet light with a peak emission wavelength of 370 nm also has a spectral component of a wavelength no less than 380 nm (visible light). Therefore, a white LED using near-ultraviolet light as an excitation light source has
20 a problem of unevenness of color. Accordingly, the present embodiment is applicable to an LED having a light emitting layer that emits near-ultraviolet light to achieve the same effects of reducing unevenness of color for the same reasons stated above. Which is to say, the present embodiment of the present invention is applicable
25 to an LED including a light emitting layer that emits light including a spectral component of a wavelength, at least, within a range of 380 nm and 780 nm to reduce unevenness of color. The application

of the present embodiment is not limited to an LED including a light emitting layer that emits blue light having a peak emission wavelength of 460 nm as described above.

[0053]

5 Fig.8 is an external perspective view illustrating a white LED module 200 including LED array chips 2 described above (hereinafter simply referred to as "an LED module 200"). The LED module 200 is attached to a lighting unit 240 (mentioned later).

[0054]

10 The LED module 200 includes a ceramics substrate 202 that is in a shape of a circle having a diameter of 5 cm and is made of aluminum nitride (AlN) and three lenses 204, 206 and 208 made of glass. A guiding depression 210 used to attach the LED module 200 to the lighting unit 240 and terminals 212 and 214 to receive a power
15 supply from the lighting unit 240 are provided in the ceramics substrate 202.

[0055]

Fig.9A is a plan view illustrating the LED module 200, Fig.9B illustrates a cross-section of the LED module 200 along a line CC
20 shown in Fig.9A, and Fig.9C is an enlargement view illustrating a portion D shown in Fig.9B.

[0056]

As shown in Figs.9A and 9B, a guiding hole (a through hole) 216 is provided in the center of the ceramics substrate 202 to attach
25 the LED module 200 to the lighting unit 240. As shown in Fig.9C, a gold plating 217 is applied to a lower surface of the ceramics substrate 202 for improving heat dissipation.

[0057]

The LED array chip 2 is mounted at a location, on an upper surface of the ceramics substrate 202, corresponding to a center of each of the lenses 204, 206 and 208 having a shape of a circle as shown in Fig.9A. In total, three LED array chips 2 are mounted on the ceramics substrate 202.

[0058]

The ceramics substrate 202 is made up of two ceramics substrates 201 and 203 each of which has a thickness of 0.5 mm and is mainly made of AlN. The ceramics substrates 201 and 203 may be made of Al_2O_3 , BN, MgO, ZnO, SiC and diamond, instead of AlN.

[0059]

The LED array chips 2 are mounted on an upper surface of the lower ceramics substrate 201. Taper through holes 215 are provided in the upper ceramics substrate 203, so as to create spaces for mounting the LED array chips 2.

[0060]

A cathode pad 218 and an anode pad 220 (shown in Fig.10B) are provided at the location, on the upper surface of the ceramics substrate 201, where each LED array chip 2 is to be mounted. Each of the cathode pad 218 and the anode pad 220 is made up of nickel (Ni) plating and then gold (Au) plating applied on copper (Cu). The LED array chip 2 is mounted on the ceramics substrate 201 in such a manner that the SiC substrate 4 is adhered to the ceramics substrate 201. Here, the power supply terminals 36 and 38 are respectively connected to the cathode pad 218 and the anode pad 220 using solder. Instead of solder, a gold bump or a silver paste may be used.

[0061]

Before being mounted on the ceramics substrate 201, the LED array chips 2 have been tested for their optical performance, such as unevenness of color, and have passed the test. The LED array chips 2 can be tested for their optical performance before being mounted because the LED array chip 2 relating to the present embodiment includes the phosphor film 48, and can emit white light by itself. Thus, it can be prevented that the LED module 300 including the LED array chips 2 is rejected due to poor optical performance of the LED array chips 2. Consequently, a ratio of accepted finished products (LED modules 300) to all finished products is improved.

[0062]

An aluminum reflection film 219 is formed on a wall of each through hole 215 provided in the upper ceramics substrate 203 and on an upper surface of the ceramics substrate 203.

[0063]

The lenses 204, 206 and 208 are adhered to the ceramics substrate 203 using an adhesive agent 221. The adhesive agent 221 may be a silicone resin, an epoxy resin or the like.

20 [0064]

The three LED array chips 2 are connected in parallel by a wiring pattern formed on the upper surface of the ceramics substrate 201.

[0065]

25 Fig. 10A is a plan view illustrating the LED module 200 after removing the lenses 204, 206 and 208. In Fig. 10A, the three LED array chips 2 are distinguished from each other by addition of marks of

A, B and C.

[0066]

As described above, the anode pad 220 and the cathode pad 218 (Fig.10B) are provided at the location, on the upper surface 5 of the ceramics substrate 201, where each of the LED array chips 2A, 2B and 2C is mounted.

[0067]

The anode pads 220 that are respectively connected to the LED array chips 2A, 2B and 2C are electrically connected to each 10 other by a wiring pattern 236. The wiring pattern 236 is connected to the positive terminal 212 at its end by a through hole 237. The cathode pads 218 that are respectively connected to the LED array chips 2A, 2B and 2C are electrically connected to each other by a wiring pattern 238. The wiring pattern 238 is connected to the negative 15 terminal 214 at its end by a through hole 239. In other words, the LED array chips 2A, 2B and 2C are connected in parallel by the wiring patterns 236 and 238.

[0068]

The LED module 200 described above is attached to the lighting 20 unit 240. The LED module 200 and the lighting unit 240 constitute a lighting apparatus 242.

[0069]

Fig.11A is a schematic perspective view illustrating the lighting apparatus 242, and Fig.11B is a bottom plan view illustrating 25 the lighting apparatus 242.

[0070]

The lighting unit 240 is, for example, fixed on a ceiling

of a room. The lighting unit 240 includes a power supply circuit (not shown in Figs.11A and 11B) that converts alternating-current power (e.g. 100 V, 50/60Hz) supplied from a commercial power source into direct-current power required for driving the LED module 200.

5 [0071]

The following part describes a construction to attach the LED module 200 to the lighting unit 240, with reference to Fig.12.

[0072]

The lighting unit 240 has a circular depression 244 in which
10 the LED module 200 is to be fitted. A bottom surface of the circular depression 244 is flat. An internal thread (not shown in Fig.12) is created, in the vicinity of an open end of the circular depression 244, on an inside wall of the circular depression 244. Flexible power supply terminals 246 and 248 and a guiding protrusion 230 protrude
15 from the inside wall of the circular depression 244, between the internal thread and the bottom surface of the circular depression 244. The power supply terminals 246 and 248 are respectively positive and negative. A guiding pin 252 is provided in the center of the bottom surface of the circular depression 244.

20 [0073]

An O-ring 254 made of silicon rubber and a ring screw 256 are used to attach the LED module 200 to the lighting unit 240. The ring screw 256 has a shape of a ring that has a substantially rectangular cross-section. An external thread (not shown in Fig.12)
25 is created on an outer surface of the ring screw 256, and a depression 258 is provided.

[0074]

The following part describes a procedure of attaching the LED module 200 to the lighting unit 240.

[0075]

To start with, the LED module 200 is fitted in the circular depression 244 in the following manner. The ceramics substrate 202 of the LED module 200 is positioned between the bottom surface of the circular depression 244 and the power supply terminals 246 and 248. The guiding pin 252 is fitted in the guiding hole 216, so as to align the center of the LED module 200 with the center of the circular depression 244. Furthermore, the guiding protrusion 230 is fitted in the guiding depression 210, so as to align the positive and negative terminals 212 and 214 with the power supply terminals 246 and 248 respectively.

[0076]

After the LED module 200 is fitted in the circular depression 244, the ring screw 256 to which the O-ring 254 has been attached is screwed into the circular depression 244 and fixed. Thus, the positive and negative terminals 212 and 214 are respectively connected to the power supply terminals 246 and 248, so that the terminals 212 and 214 are electrically connected to the terminals 246 and 248 reliably. In addition, the substantially entire lower surface of the ceramics substrate 202 is connected to the flat bottom surface of the circular depression 244. This enables heat generated in the LED module 200 to be effectively conducted to the lighting unit 240, thereby improving a cooling effect of the LED module 200. Here, silicone grease may be applied to the lower surface of the ceramics substrate 202 and the bottom surface of the circular

depression 244 to further improve the heat conduction efficiency from the LED module 200 to the lighting unit 240.

[0077]

When power is supplied to this lighting apparatus 242 from
5 a commercial power source, the LEDs 6 emit blue light in each LED array chip 2. Here, part of the blue light is converted into yellow light by the phosphor within the phosphor film 48. The blue light and the yellow light mix together, to generate white light. The white light is emitted through the lenses 204, 206 and 208.

10 When an electric current of 150 mA is applied to the LED module 200, a total luminous flux of 800 lm, an on-axis luminous intensity of 1500 cd, and an emission spectrum shown in Fig.13 are observed.

[0078]

15 It should be noted that the present embodiment includes the following modification examples.

(1) According to the above embodiment, the removed multilayer portion includes all of the layers composing the semiconductor multilayer film (see step C in Fig.4). However, the
20 above embodiment is not limited to such. It is acceptable as long as the removed multilayer portion includes the layers from an outmost layer (the n-GaN contact layer 118) to a conductive layer between the light emitting layer 114 and the SiC substrate 104 (the n-GaN clad layer 112). As long as this condition is satisfied, the phosphor
25 film can be formed at a large thickness not only on the upper surface of the semiconductor multilayer film made up of the layers but also on the side surfaces of the semiconductor multilayer film which is

created by the removed multilayer portion. As a result, unevenness of color can be reduced as described above.

(2) According to the above embodiment, the SiC substrate is used as a substrate on which the semiconductor multilayer film made up of the layers from the n-AlGaIn buffer layer to the p-GaN contact layer are formed by crystal growth. This is because the SiC substrate has a higher heat conductivity than copper and aluminum, and can efficiently conduct heat generated by the light emitting layer to the ceramics substrate which is a printed-wiring board and on which the LED array chips are mounted. The SiC substrate may be replaced with one of an AlN substrate, a GaN substrate, a BN substrate and an Si substrate as they similarly have a high heat conductivity.

[0079]

Alternatively, the above embodiment may be realized by employing a generally used sapphire substrate, which has a slightly lower heat conductivity.

(3) According to the above embodiment, the LED array chip includes the 35 LEDs (light emitting elements), and is a square approximately 2 mm on its side. However, the above embodiment is not limited to such. The LED array chip may include any number of LEDs (light emitting elements).

[0080]

Alternatively, the above embodiment may be realized by an LED chip constituted by one LED (light emitting element), instead of the LED array chip. If such is the case, the exposed portion is formed so as to surround each LED in the step C of the manufacturing method.

[INDUSTRIAL APPLICABILITY]

[0081]

As describe above, a semiconductor light emitting device
5 of the present invention is applicable to the field of lighting
apparatuses that require a light emitting device used for a lighting
apparatus to be tested for its optical performance, for example,
unevenness of color, before being mounted on the lighting apparatus.

10 [BRIEF DESCRIPTION OF THE DRAWINGS]

[0082]

Fig.1A is a perspective view illustrating an LED array chip,
and Fig.1B is a plan view illustrating the LED array chip.

Figs.2A and 2B are cross-sectional views illustrating a
15 part of the LED array chip.

Fig.3A is a bottom plan view illustrating the LED array
chip, Fig.3B is a plan view illustrating an LED in the LED array
chip, and Fig.3C illustrates connections in the LED array chip.

Figs.4A to 4C illustrate part of a manufacturing method
20 for the LED array chip.

Figs.5D to 5F illustrate part of the manufacturing method
for the LED array chip.

Figs.6G to 6I illustrate part of the manufacturing method
for the LED array chip.

25 Figs.7J to 7M illustrate part of the manufacturing method
for the LED array chip.

Fig.8 is a perspective view illustrating an LED module.

Fig.9A is a plan view illustrating the LED module, Fig.9B illustrates a cross-section of the LED module along a line CC shown in Fig.9A, and Fig.9C is an enlargement view illustrating a portion D shown in Fig.9B.

5 Fig.10A illustrates the LED module after removing a lens, and Fig.10B illustrates a pad pattern formed on a ceramics substrate constituting the LED module.

Fig.11A is a perspective view illustrating a lighting apparatus, and Fig.11B is a bottom plan view illustrating the lighting
10 apparatus.

Fig.12 is a perspective exploded view illustrating the lighting apparatus.

Fig.13 shows an emission spectrum of the lighting apparatus.

15 [DESCRIPTION OF CHARACTERS]

[0083]

4 SiC substrate

7 exposed portion

10 DBR layer composed of 30 periods of n-AlGa_N/Ga_N

20 14 multiple quantum well light emitting layer composed of six periods of InGa_N/Ga_N

48 phosphor film

[DOCUMENT] Abstract

[SUMMARY]

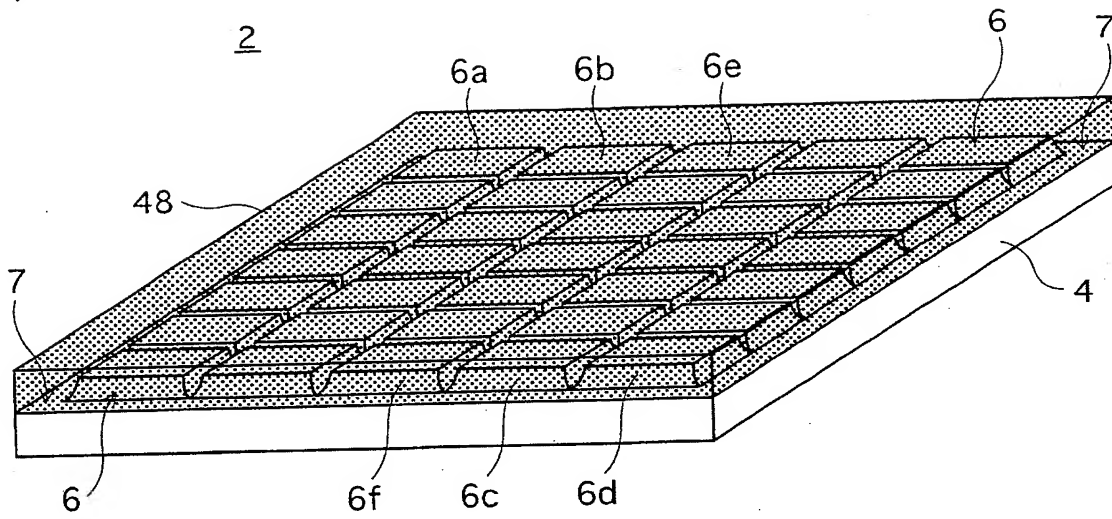
[PROBLEM] To provide a semiconductor light emitting device that can improve the yield of acceptable finished products without an increase
5 in the number of parts or manufacturing steps.

[MEANS TO SOLVE THE PROBLEM] An LED array chip 2 (semiconductor light emitting device) includes a substrate 7, an LED array composed of 35 LEDs 6 that have been formed on the substrate 7 by crystal growth, an exposed portion 7 formed so as to surround the LED array, and
10 a phosphor film 48 that covers the exposed portion 7 and the LED array.

[SELECTED FIGURE] Fig.1

[DOCUMENT] Drawings
[FIG. 1]

(a)



(b)

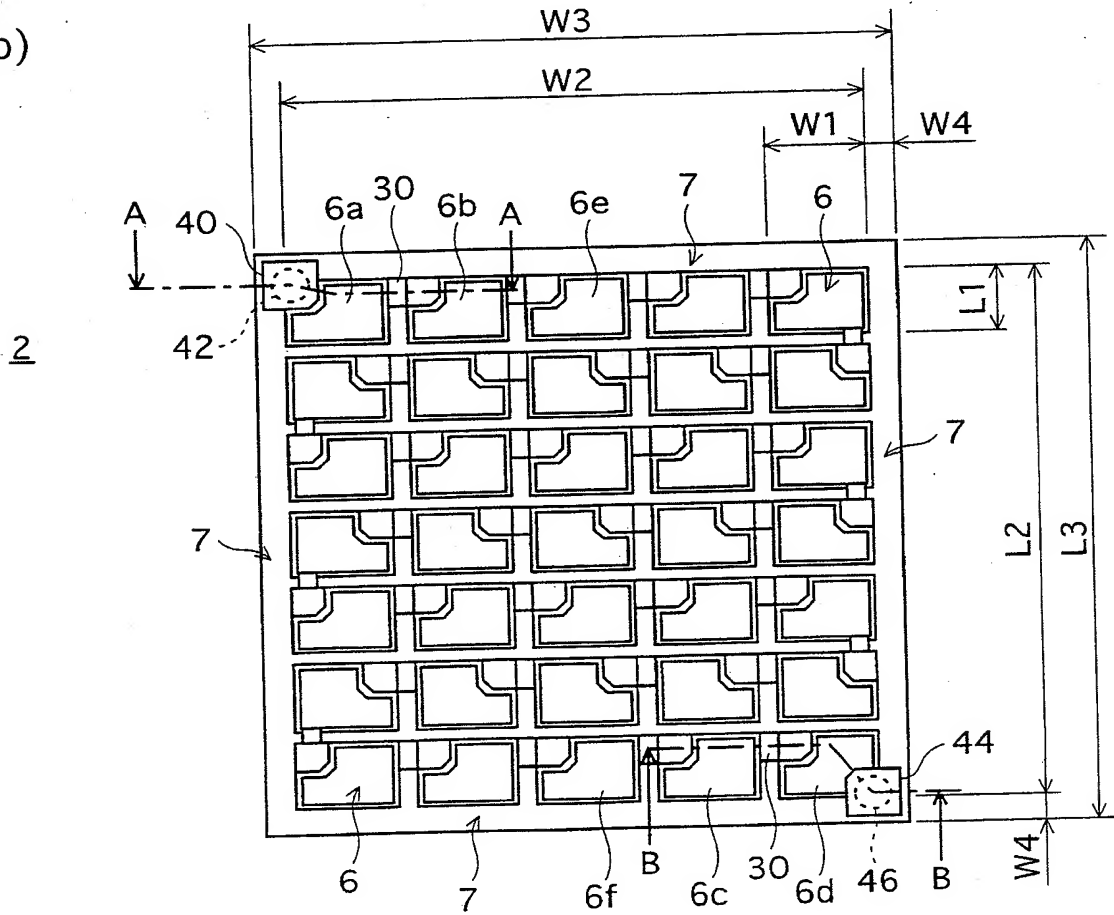
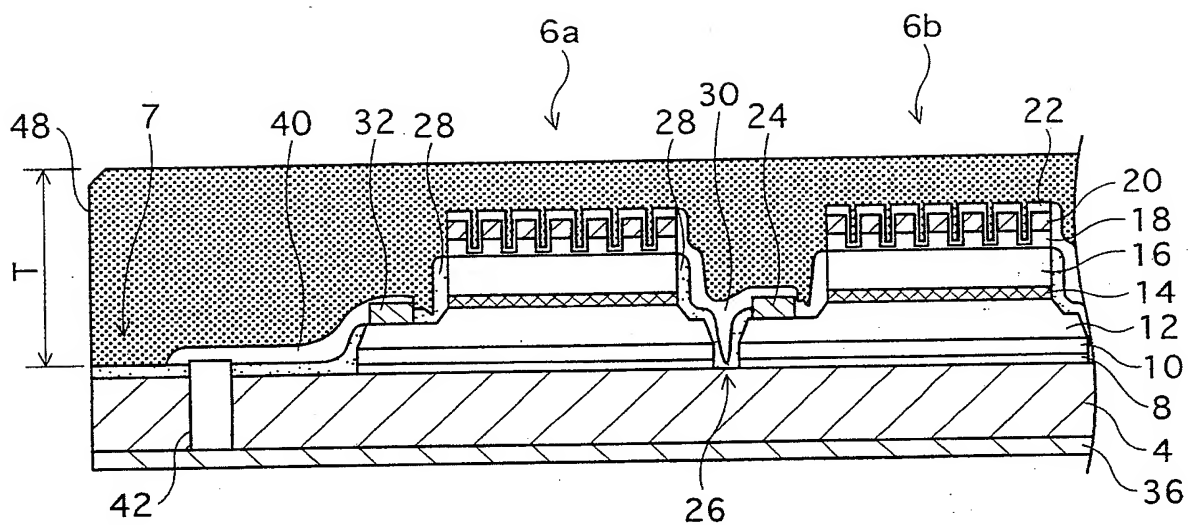


FIG. 2

(a)



(b)

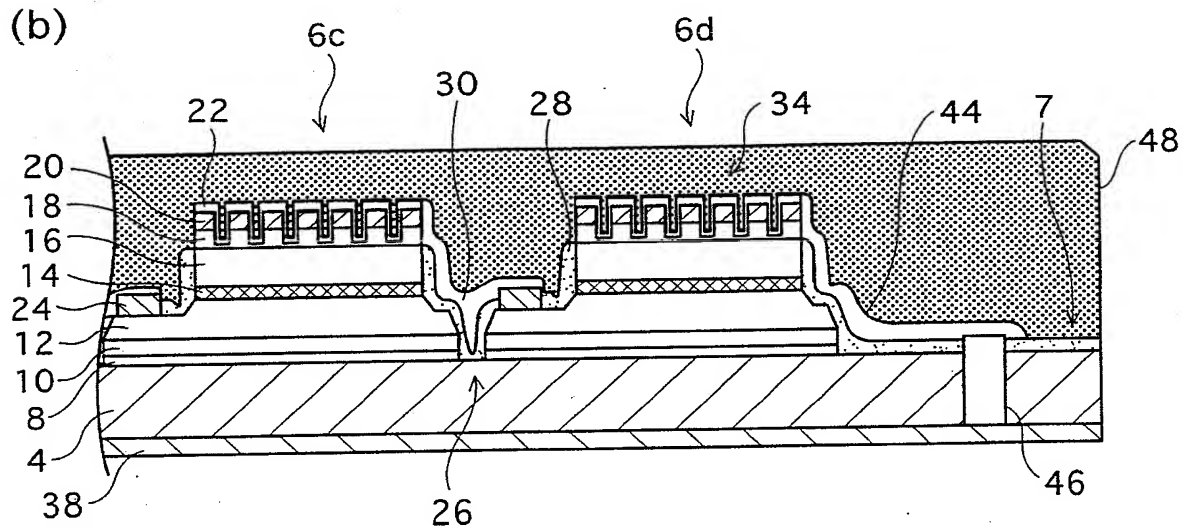


FIG. 3

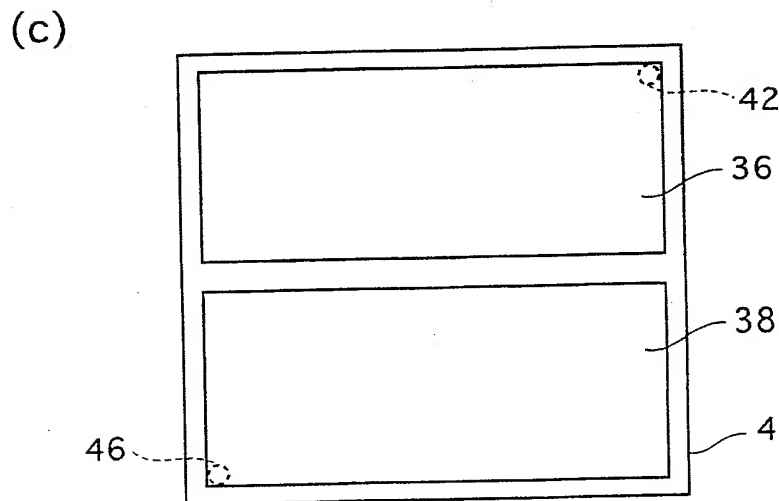
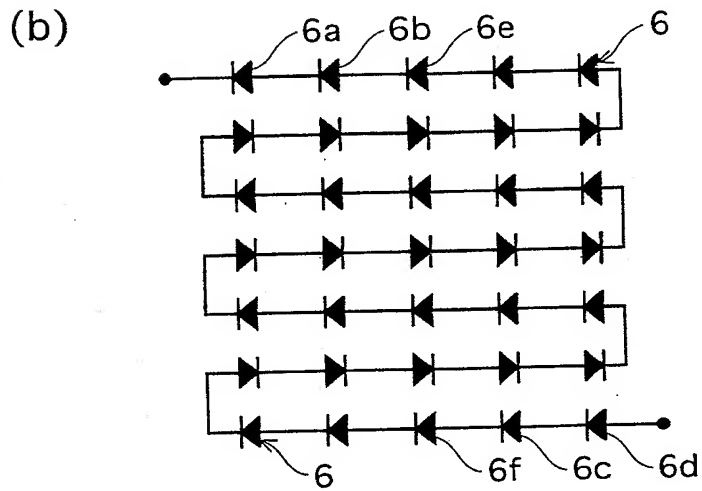
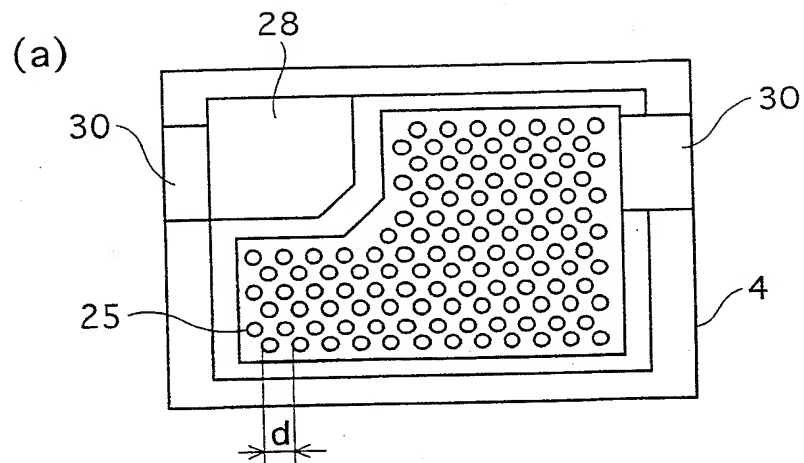
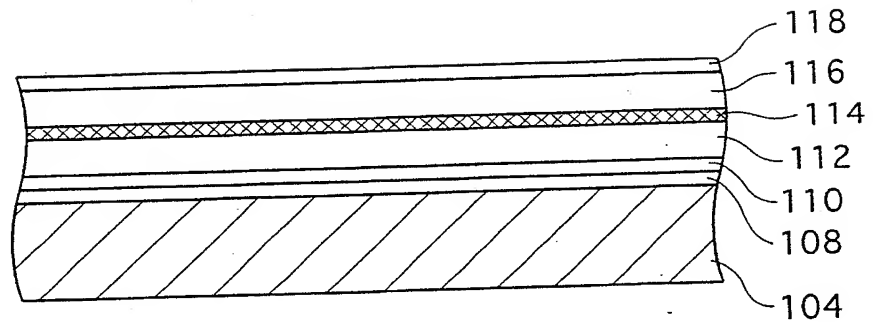
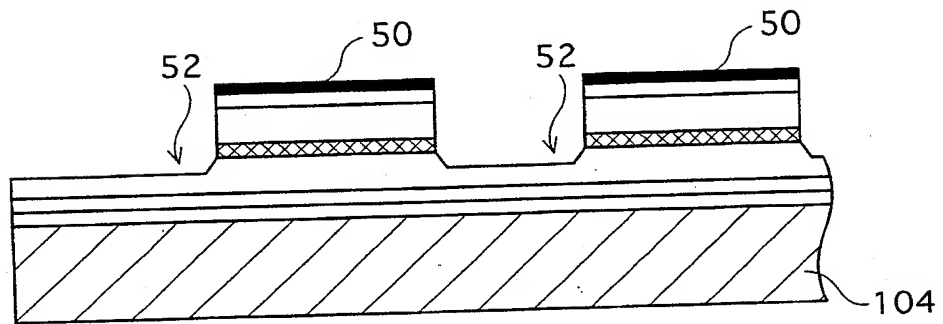


FIG. 4

(a)



(b)



(c)

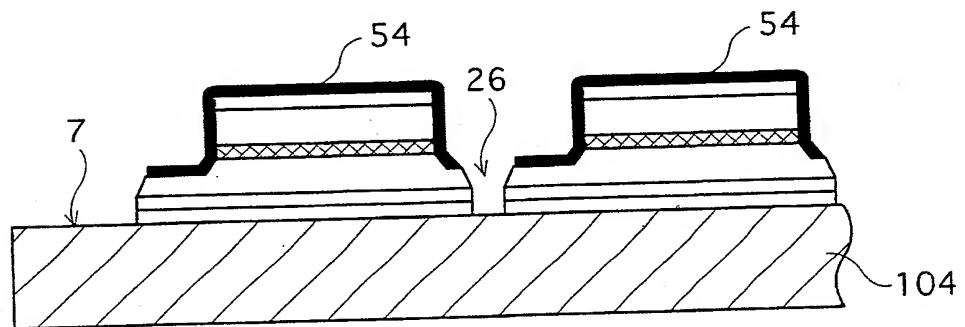
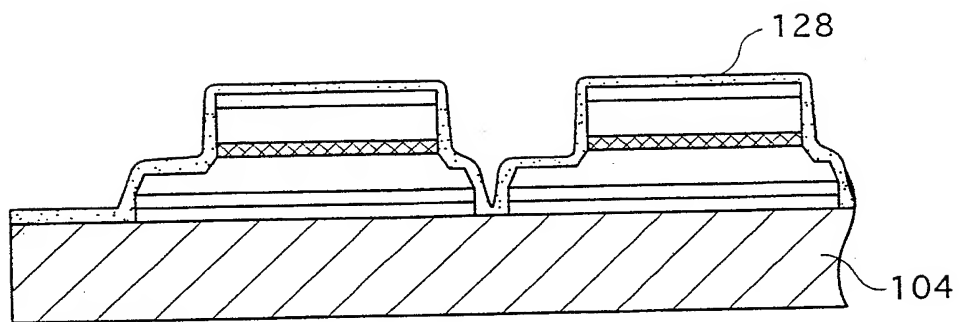
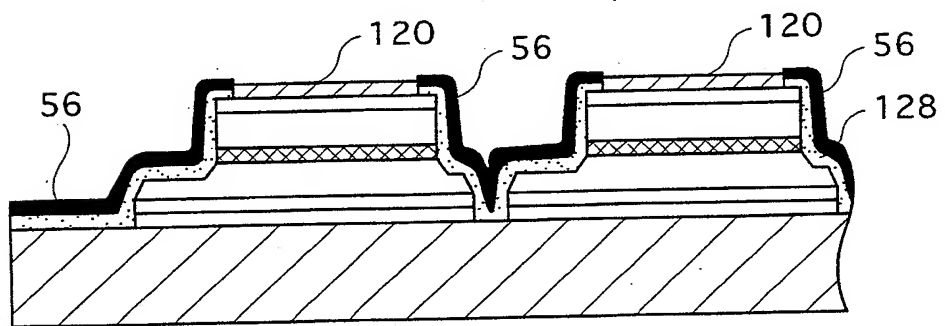


FIG. 5

(d)



(e)



(f)

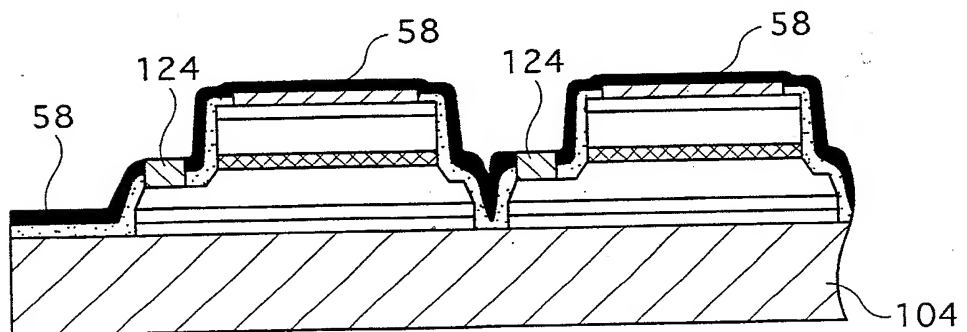
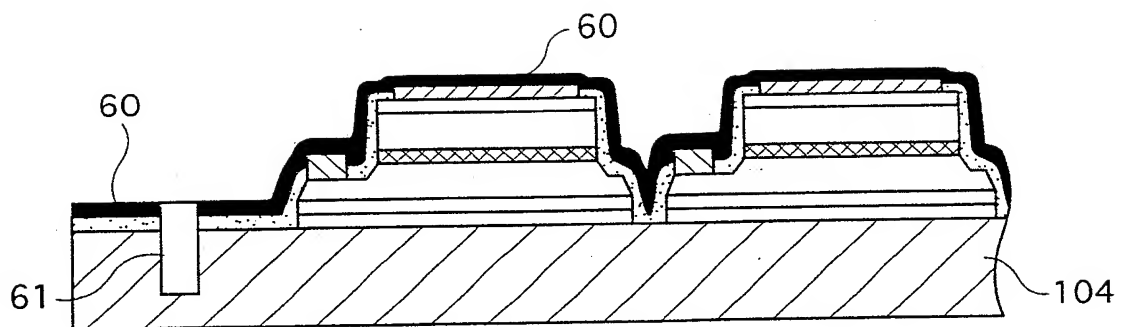
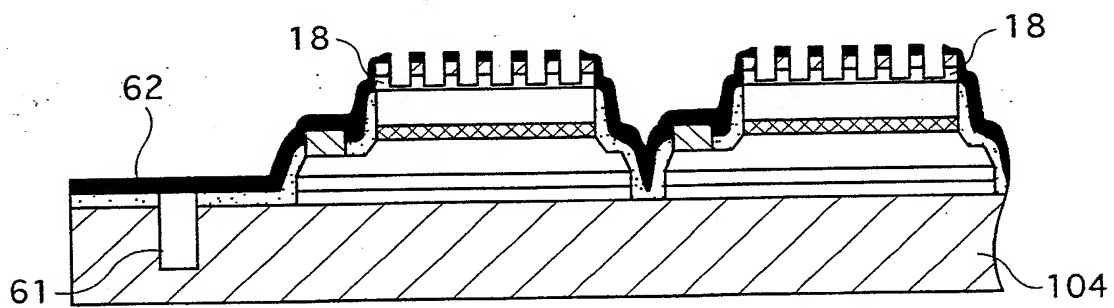


FIG. 6

(g)



(h)



(i)

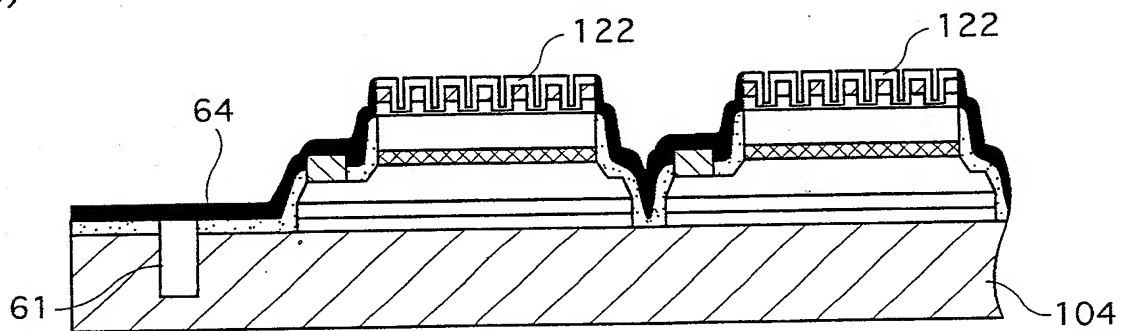
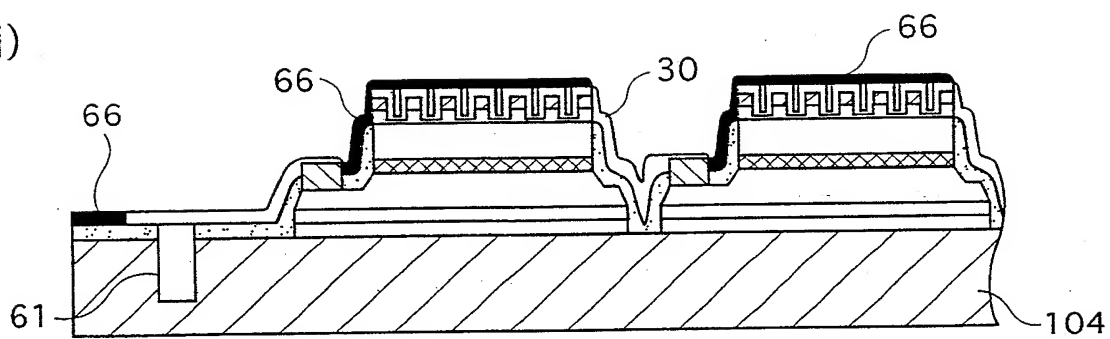
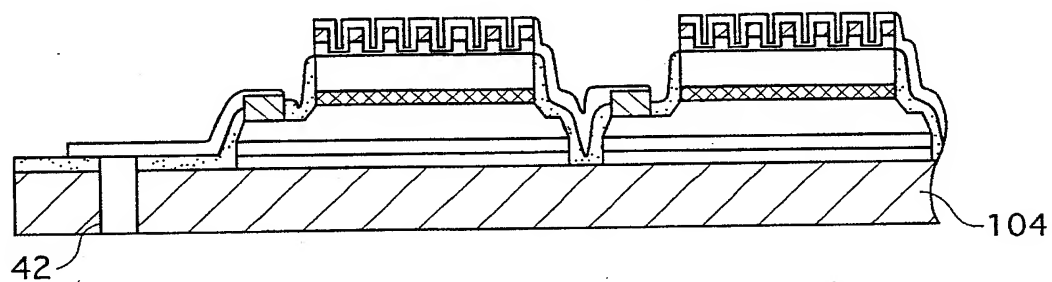


FIG. 7

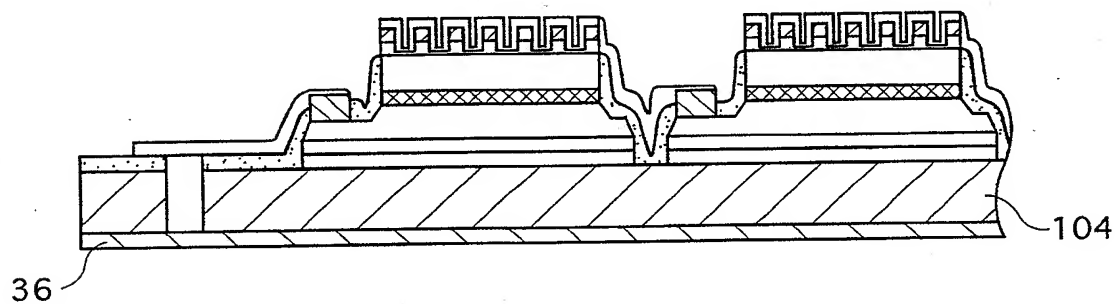
(j)



(k)



(l)



(m)

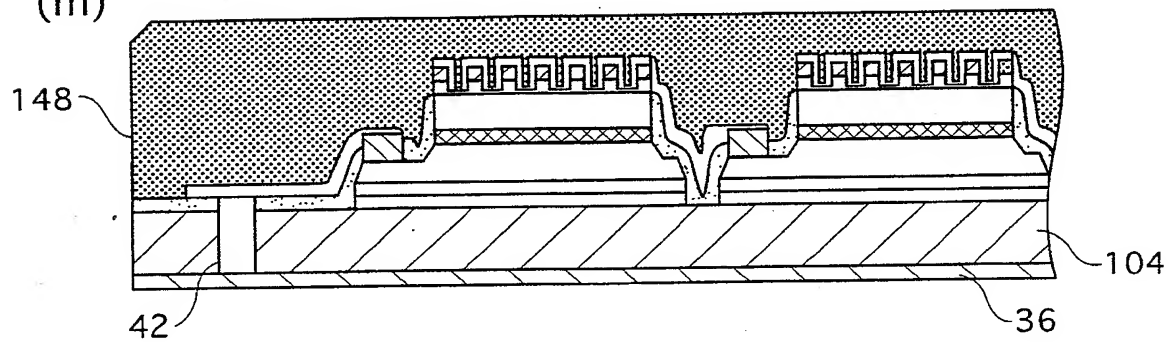


FIG. 8

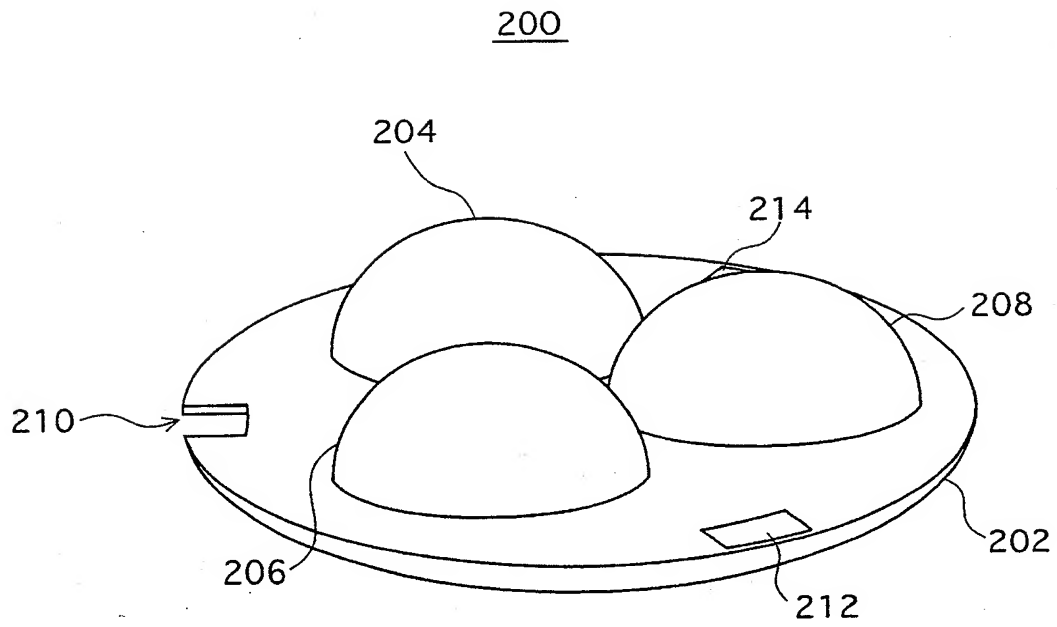


FIG. 9

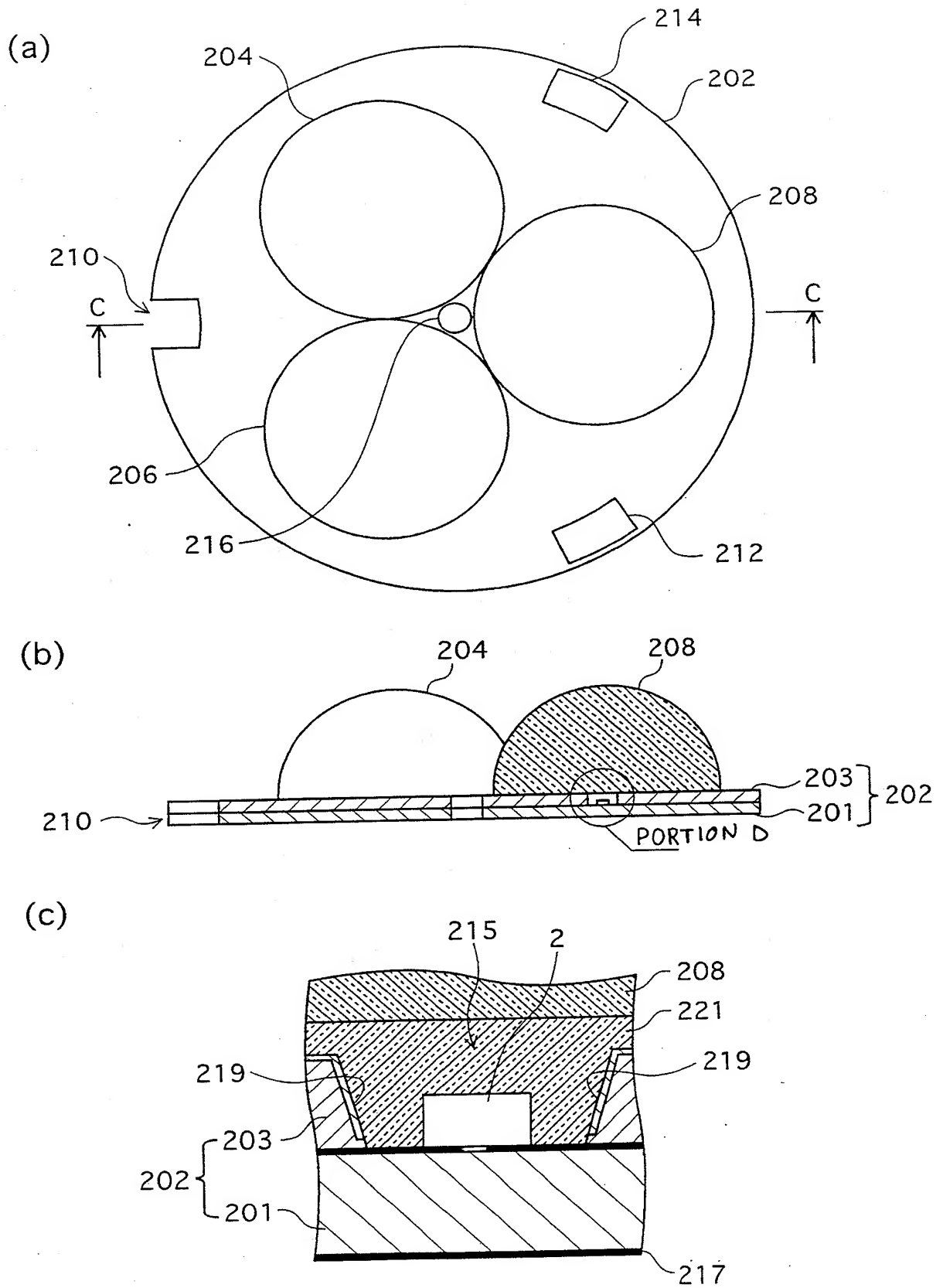
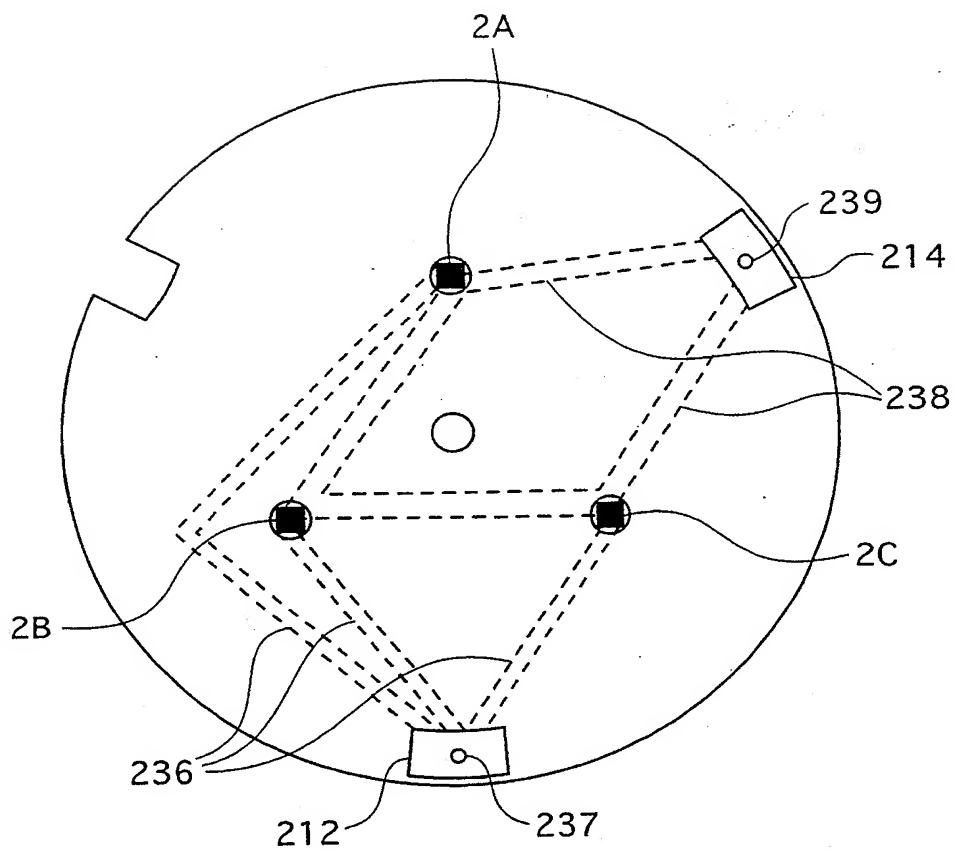


FIG. 10

(a)



(b)

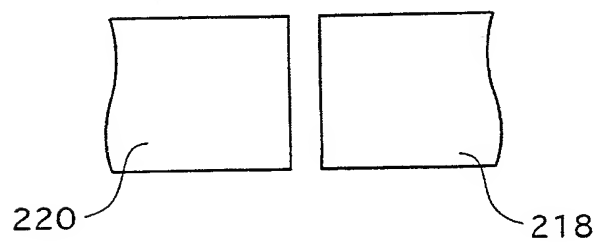
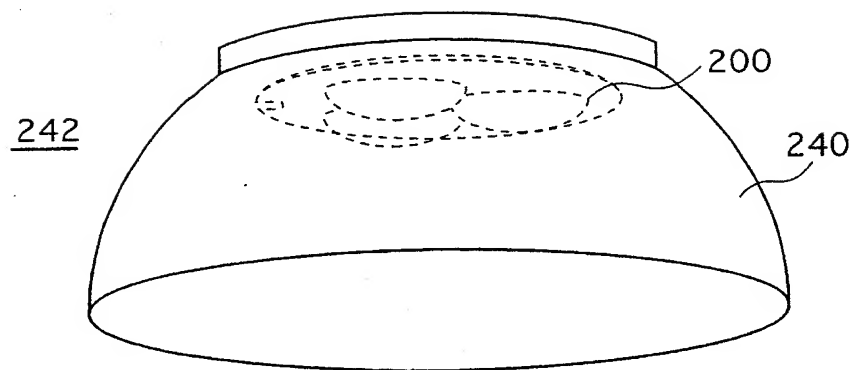


FIG. 11

(a)



(b)

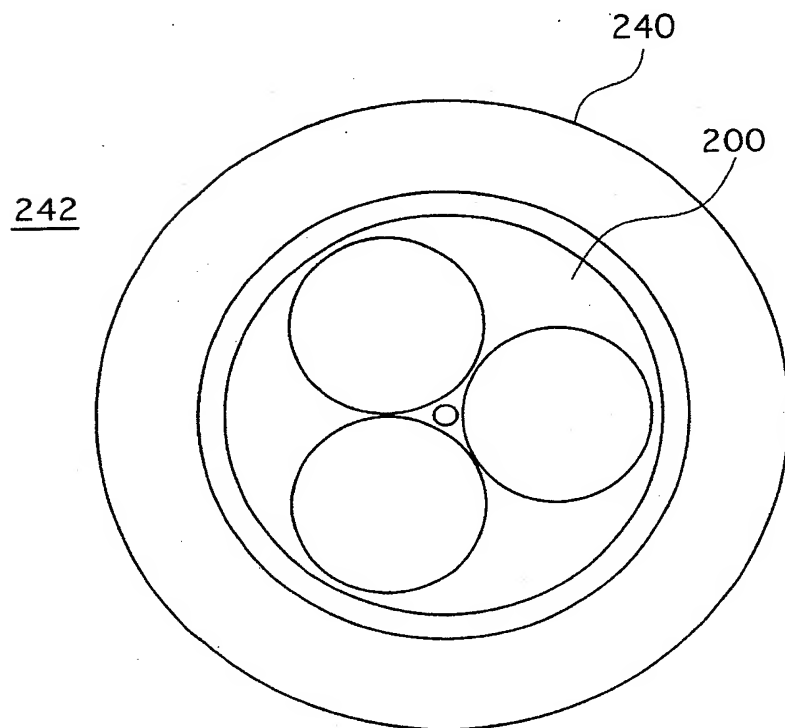


FIG. 12

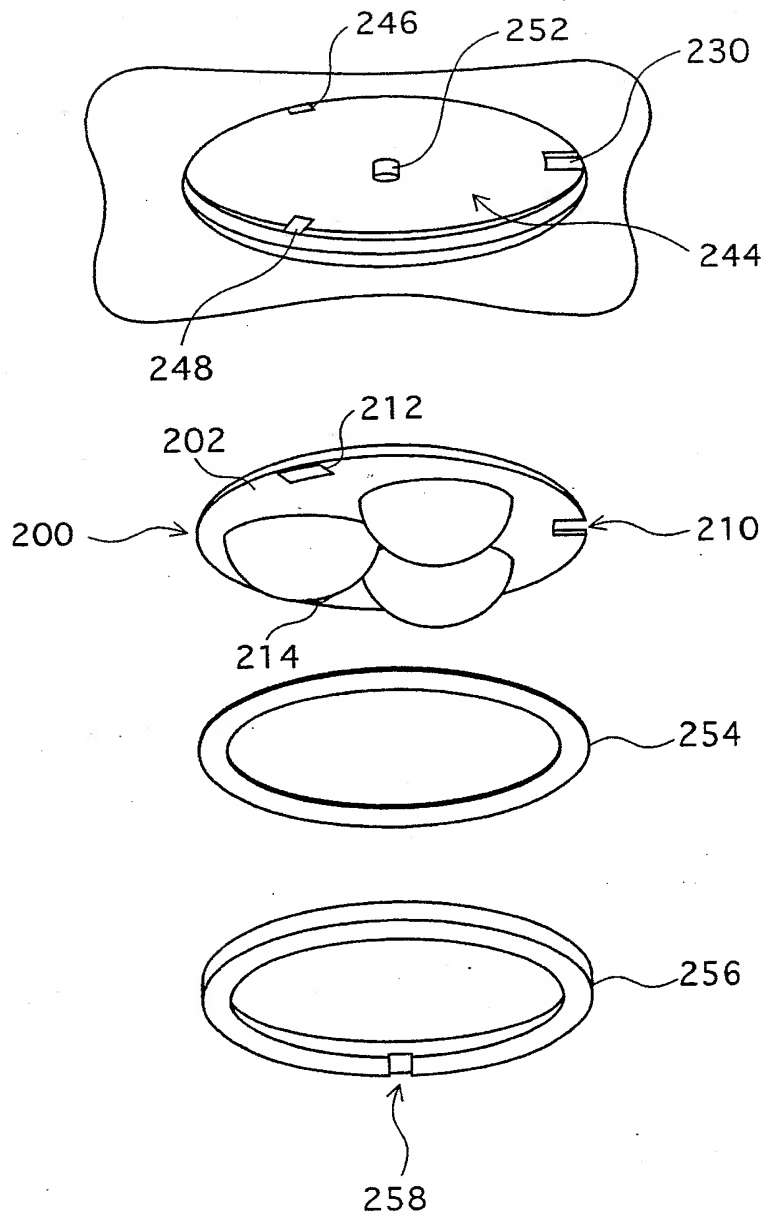


FIG. 13

